a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of [a] the first conductivity type; and

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming [an] the extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and [a] the pocket dopant diffused layer of the second conductivity type, which is located under the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively,

wherein the pocket dopant diffused layer includes a segregated part that has been formed through segregation of the heavy ions.

8. (Amended) A method for fabricating a semiconductor device according to claim 6, further comprising the steps of:

forming a sidewall spacer on side faces of the gate electrode after the third step has been performed;

implanting ions of a [third] second dopant into the semiconductor region using the gate electrode and the sidewall spacer as a mask, thereby forming a third ion implanted layer of the first conductivity type; and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer of the first conductivity type, which is located outside of the extended high-concentration dopant diffused layer, has a junction deeper than that of the extended high-concentration dopant diffused layer and has been formed through diffusion of a second dopant.

9. (Amended) A method for fabricating a semiconductor device according to claim 8, wherein the heavy ions are implanted at such an implant energy as forming an amorphous/crystalline interface, through implantation of the heavy ions, at a level equal to or deeper than a range of the first dopant and shallower than a range of the [first] second dopant.